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11-30-01

PTO/SB/05 (11-00)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. 1.53(b))

Attorney Docket No.	VAO-004.01
First Inventor	Downey, Daniel F.
Title	Athermal Annealing With Rapid Thermal Annealing System and Method
Express Mail Label No.	EL-719917836 US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. [X] Fee Transmittal Form (e.g., PTO/SB/17) *(Submit an original and a duplicate for fee processing)*
2. [ ] Applicant claims small entity status. See 37 CFR 1.27.
3. [X] Specification [*Total Pages* 20] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to sequence listing, a table, or a computer program listing appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
4. [X] Drawing(s) (*35 U.S.C.113*) [*Total Sheets* 7]
5. Oath or Declaration [*Total Pages* 27]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63 (d)) *(for a continuation/divisional with Box 18 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
6. [ ] Application Data Sheet. See 37 CFR 1.76

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7. [ ] CD-ROM or CD-R in duplicate, large table or Computer Program *(Appendix)*
8. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Form (CRF)
   b. Specification Sequence Listing on:
      i. [ ] CD-ROM or CD-R (2 copies); or
      ii. [ ] paper
   c. [ ] Statements verifying identity of above copies

ACCOMPANYING APPLICATIONS PARTS

9. [X] Assignment Papers (cover sheet & document(s))
10. [ ] 37 C.F.R.§3.73(b) Statement [ ] Power of Attorney *(when there is an assignee)*
11. [ ] English Translation Document *(if applicable)*
12. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
13. [ ] Preliminary Amendment
14. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
15. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
16. [ ] Request and Certification under 35 U.S.C. 122 (b)(2)(B)(i). Applicant must attach form PTO/SB/35 or its equivalent.
17. [X] Other: Request for Non-Publication

18. If a CONTINUING APPLICATION, *check appropriate box, and supply the requisite information below and in a preliminary amendment, or in an Application Data Sheet under 37 CFR 1.76:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: ____ / ____

Prior application information: *Examiner* ____ *Group / Art Unit:* ____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 5b, is considered a part of the disclosure of the accompanying or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

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Name					
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City		*State*		*Zip Code*	
Country		*Telephone*		*Fax*	

Name (Print/Type)	Kevin A. Oliver	*Registration No. (Attorney/Agent)*	42,049
Signature	Kevin A Oliver	*Date*	11/28/01

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Terrill Williams

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FEE TRANSMITTAL for FY 2002

Patent fees are subject to annual revision.

TOTAL AMOUNT OF PAYMENT	($) 780.00

Complete if Known	
Application Number	
Filing Date	November 28, 2001
First Named Inventor	Downey, Daniel F.
Examiner Name	
Group / Art Unit	
Attorney Docket No.	VRO-004.01

METHOD OF PAYMENT (check one)

1. ☒ The Commissioner is hereby authorized to charge indicated fees and credit any over payments to:

Deposit Account Number: 06-1448

Deposit Account Name:

☐ Charge Any Additional Fee Required Under 37 CFR 1.16 and 1.17

☐ Applicant claims small entity status. See 37 CFR 1.27

2. ☐ Payment Enclosed:

☐ Check ☐ Credit card ☐ Money Order ☐ Other

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
101	740	201	370	Utility filing fee	740.00
106	330	206	165	Design filing fee	
107	510	207	255	Plant filing fee	
108	740	208	370	Reissue filing fee	
114	160	214	80	Provisional filing fee	

SUBTOTAL (1) ($) 740.00

2. EXTRA CLAIM FEES

			Extra Claims		Fee from below	=	Fee Paid
Total Claims	17	20 =	0	X		=	0
Independent Claims		- ** =	0	X		=	0
Multiple Dependent				X		=	0

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
103	18	203	9	Claims in excess of 20
102	84	202	42	Independent claims in excess of 3
104	280	204	140	Multiple dependent claim, if not paid
109	84	209	42	** Reissue independent claims over original patent
110	18	210	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) !Undefined Bookmark, TEXT130

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FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
105	130	205	65	Surcharge - late filing fee or oath	
127	50	227	25	Surcharge - late provisional filing fee or cover sheet.	
139	130	139	130	Non-English specification	
147	2,520	147	2,520	For filing a request for reexamination	
112	920*	112	920*	Requesting publication of SIR prior to Examiner action	
113	1,840*	113	1,840*	Requesting publication of SIR after Examiner action	
115	110	215	55	Extension for reply within first month	
116	400	216	200	Extension for reply within second month	
117	920	217	460	Extension for reply within third month	
118	1,440	218	720	Extension for reply within fourth month	
128	1,960	228	980	Extension for reply within fifth month	
119	320	219	160	Notice of Appeal	
120	320	220	160	Filing a brief in support of an appeal	
121	280	221	140	Request for oral hearing	
138	1,510	138	1,510	Petition to institute a public use proceeding	
140	110	240	55	Petition to revive – unavoidable	
141	1,280	241	640	Petition to revive – unintentional	
142	1,280	242	640	Utility issue fee (or reissue)	
143	460	243	230	Design issue fee	
144	620	244	310	Plant issue fee	
122	130	122	130	Petitions to the Commissioner	
123	50	123	50	Processing fee under 37 CFR 1.17 (q)	
126	180	126	180	Submission of Information Disclosure Stmt	
581	40	581	40	Recording each patent assignment per property (times number of properties)	40.00
146	740	246	370	Filing a submission after final rejection (37 CFR § 1.129(a))	
149	740	249	370	For each additional invention to be examined (37 CFR § 1.129(b))	
179	740	279	370	Request for Continued Examination (RCE)	
169	900	169	900	Request for expedited examination of a design application	
				Other fee (specify) ____	

*Reduced by Basic Filing Fee Paid SUBTOTAL (3) ($) 40.00

SUBMITTED BY				Complete *(if applicable)*	
Name (Print/Type)	Kevin A. Oliver	*Registration No. Attorney/Agent)*	42,049	*Telephone*	617-832-1241
Signature	Kevin A. Oliver			*Date*	November 28, 2001

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Terrill Williams

Terrill Williams

09995447.112801

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REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	Downey, Daniel F.
	Title	ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD
	Atty Docket Number	VRO-004.01

I hereby certify that the invention disclosed in the attached application **has not and will not be** the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

11/28/2001
Date

Kevin A. Oliver
Signature

Kevin A. Oliver 42,049
Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing.**

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

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Terrill Williams

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FROM: Office of Initial Patent Examination

SUBJECT: Fee Due $ 740

APPLICATION NUMBER: _____

A fee is due for the attached document submitted to the U. S. Patent and Trademark Office for the following reason. Please check the application for the appropriate authorization to charge a deposit account. If an authorization is present, please charge the appropriate fee. If an authorization is not present, notify the applicant of the fee deficiency.

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Fee Due	amount	=$ _____

If you have any questions, please contact Cynthia Streater at 703-306-5430 or Eleanor Kurtz at 703-308-3642.

Terminal Operator _____

Docket No.: VRO-004.01

APPLICATION

FOR

UNITED STATES LETTERS PATENT

ENTITLED

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

TO WHOM IT MAY CONCERN:

BE IT KNOWN THAT (1) DANIEL F. DOWNEY and (2) EDWIN A. AREVALO of (1) 8 Ryan Road Gloucester, MA 01930, and (2) 34 Miriam Road, Waltham, MA 02451, invented certain new and useful improvements entitled as set forth above of which the following is a specification:

PATENT GROUP
FOLEY, HOAG & ELIOT LLP
ONE POST OFFICE SQUARE
BOSTON, MA 02109-2170
TEL: 617-832-1000
FAX: 617-832-7000

Docket No.: VRO-004.01

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

BACKGROUND

(1) Field

The disclosed methods and systems relate generally to annealing processes, and more particularly to athermal annealing.

(2) Description of Relevant Art

Conventional ion implantation systems include ionizing a dopant material such as boron, accelerating the ions to form an ion beam having a given energy level, and directing the ion beam energy at a semiconductor surface or wafer to introduce the dopant material to the semiconductor and alter the conductivity properties of the semiconductor. Once the ions are embedded into the crystalline lattice of the semiconductor, the ions can be activated using a process known as rapid thermal annealing (RTA) or rapid thermal process (RTP). During RTA, the semiconductor can be introduced to a furnace to heat the semiconductor at a prescribed temperature and for a prescribed time. RTA can also cure defects in the crystalline structure that can be caused by the ion implantation.

The processes of ion implantation and RTP contribute to the depth of the implanted region, known as the junction depth.

Those of ordinary skill in the art recognize that the junction depth from ion implantation is based on the energy of the ions implanted into the semiconductor. Accordingly, shallow implanted regions can be formed using low-energy ion beams. Unfortunately, traditional methods of RTA include raising the temperature of the silicon to ranges nearing 1100-1200 degrees Celsius, which can approach the melting temperature of the silicon. Accordingly, RTA can further increase the implanted junction depth as high temperatures of the RTA process cause further diffusion of the implanted region.

The increase in junction depth can be particularly troublesome when considered with respect to a continuing and expanding demand for smaller devices, and hence shallower junction depths. It is anticipated that the present methods and systems that combine ion implantation solely with traditional RTA may not satisfy the demand for shallower junctions.

SUMMARY

The disclosed methods and systems include features for annealing a semiconductor structure that include subjecting the semiconductor structure to an oscillating magnetic field and applying a low temperature rapid thermal annealing (LTRTA) process to the semiconductor structure. The electromagnetic field can be a time-varying electromagnetic field that can be

provided by, for example, a signal having a frequency in the microwave or the radio frequency (RF) bands.

In one embodiment, the LTRTA can include exposing the semiconductor to a temperature less than approximately 800 degrees Celsius, while in another embodiment, the temperature can be greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius. The RTA can be performed in a furnace or another annealing device.

For the disclosed methods and systems, the LTRTA can be performed either before or after the application of electromagnetic field or energy.

The methods and systems can accordingly be implemented with and/or applied to ion implantation systems where dopant material ions can be implanted into a semiconductor structure or wafer. The semiconductor wafer can include silicon or Gallium Arsenide, for example. The dopant can be any one of an n-type dopant and a p-type dopant.

Other objects and advantages will become apparent hereinafter in view of the specification and drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is one embodiment of a system and method for performing Electromagnetic Induction Heating (EMIH) annealing using microwave frequencies;

FIG. 2A is a TM011 magnetic field pattern;

FIG. 2B is a TM111 magnetic field pattern;

FIG. 3 is one embodiment of a radio frequency system and method for performing EMIH annealing;

FIG. 4 displays a relationship between power absorption and conductivity;

FIG. 5 displays a relationship between conductivity and temperature for various dopant levels;

FIG. 6 includes a SEMATECH barrier curve for evaluating improvements in anneal and doping technology; and,

FIG. 7 provides a SIMS profile for as-implanted and microwave spike annealed plasma doped (PLAD) samples.

DESCRIPTION

To provide an overall understanding, certain illustrative embodiments will now be described; however, it will be understood by one of ordinary skill in the art that the systems and methods described herein can be adapted and modified to provide systems and methods for other suitable applications and that other additions and modifications can be made without departing from the scope of the systems and methods described herein.

Unless otherwise specified, the illustrated embodiments can be understood as providing exemplary features of varying detail of certain embodiments, and therefore features, components,

modules, and/or aspects of the illustrations can be otherwise combined, separated, interchanged, and/or rearranged without departing from the disclosed systems or methods.

During ion implantation, the implanted regions can be damaged when the accelerated, energized dopant ions collide with the host or silicon surface, displacing silicon atoms from their original lattice sites. Although the dopant ions can be in high-energy non-equilibrium positions in the silicon lattice, the dopant ions are not electrically active. A rapid thermal annealing (RTA) process can provide energy to the silicon and dopant ions to allow movement of the ions to equilibrium positions, thereby also repairing the implantation damage by restoring crystallographic order. Unfortunately, the RTA process that exposes the semiconductor surface to high temperatures in the range of 1000-1200 degrees Celsius, often also causes dopant redistribution or diffusion. RTA for certain implant doses can increase junction depths to be significantly deeper than, for example, the as-implanted range.

For example, with regard to transistor devices, the consequences of a continued demand for small devices can be anticipated to include a limiting of lateral diffusion under the gate and a maintenance of high concentration of dopant material in a shallow source/drain extension region. Accordingly, the disclosed methods and systems include a combination of athermal

annealing and rapid thermal annealing (RTA) to obtain a very shallow junction with a device having a low sheet resistance. The methods and systems accordingly utilize electromagnetic fields to induce current flow through a silicon wafer and cause ohmic collisions between high energy electrons and the silicon lattice structure to provide rapid heating of the silicon from within the structure, as opposed to RTA that applies high temperatures to the structure surface. The athermal heating of the silicon, referred to herein as Electromagnetic Induction Heating (EMIH), provides energy to activate the dopant that can provide greater activation than a method or system using RTA (also referred to and known as RTP). Low temperature RTA (LTRTA), understood herein to be temperatures less than approximately 800 degrees Celsius, but for the illustrated embodiments, preferably between approximately 500 degrees Celsius and approximately 800 degrees Celsius, can also be performed before and/or after the EMIH to further repair the silicon structure and minimize diffusion. LTRTA can be performed at a temperature, and for a time period, that can be significantly less than generally associated with processes that only use RTA annealing for dopant activation and crystallographic defect curing. Those of ordinary skill in the art recognize that merely using LTRTA can fail to activate the dopant and hence can result in a large sheet resistance. Accordingly, by combining the

athermal annealing to provide dopant activation and the LTRTA (approximately 500-800 degrees Celsius) RTA to cure the structural defects, the dopant material can be activated, the lattice structure can be repaired, and differences between the as-implanted junction depth and the post-annealing junction depth can be minimized when compared to methods that use only RTA.

EMIH can be understood as a unique application of Faraday's and Ampere's laws. As a silicon wafer is exposed to oscillating magnetic fields, electrons are induced to flow within the wafer. As the electrons collide with the lattice, they release energy that heats the silicon wafer. This athermal, internal heating via EMIH can be compared to, for example, RTA that generally exposes the wafer to a furnace at a prescribed temperature and causes the silicon to be heated from the outside surface in, thereby raising a possibility of silicon melt.

Those with ordinary skill in the art recognize that for highly conducting materials such as copper, induced currents re-induce a magnetic field that partially or completely interferes with the incident electromagnetic field. Alternately, insulating materials such as quartz lack free carriers and hence preclude any flow of current, thereby allowing the incident field to penetrate the material. Semiconductors such as silicon can have properties of conductors and insulators, and thus can have a

potential for significant electromagnetic field penetration that can induce substantial currents throughout the wafer volume.

In the disclosed methods and systems, electromagnetic fields can be induced by subjecting the silicon sample to electromagnetic energy having frequencies in the radio frequency (RF) and microwave ranges, although those with ordinary skill in the art will recognize that the methods and systems are not limited to these frequency ranges, and other methods of inducing electromagnetic energy can be used. The rapid, internal ohmic heating of the wafers caused by the induced currents in the silicon wafer can cause dopant activation that can be more effective than the activation that can be caused by the surface heating provided by RTA.

Referring now to FIG. 1, there is one embodiment of a microwave system that includes a resonant cavity having a radius of seventeen centimeters, and a height that can be adjusted between fifteen and forty-five centimeters for tuning to specific microwave modes. A magnetron source can provide a maximum three thousand watts of power at 2.45GHz. One of ordinary skill in the art will recognize that various modes can be provided by a system according to FIG. 1, including but not limited to the well-known TM011 and TM111 modes. FIGs. 2A and 2B provide magnetic field patterns in the FIG. 1 microwave cavity for the TM011 and TM111 modes, respectively.

Referring to FIG. 3, there is a RF embodiment of the disclosed methods and systems that utilizes an exciting RF magnetic flux with a spiral copper antenna. A power supply matched through an L-type matching network can provide up to one-thousand Watts at a fixed 13.56MHz frequency. In the FIG. 3 system, a silicon wafer can be positioned on a ceramic chuck two-and-a-half centimeters below the coil windings in an extreme near field of the antenna. In the illustrated system, the ceramic chuck can be heated to one-hundred fifty degrees Celsius.

Those with ordinary skill in the art will recognize that the exemplary electromagnetic induction systems of FIGs. 1 and 3 are merely illustrative and the implementation thereof is not limited to the embodiments or characteristics provided herein. Furthermore, although FIGs. 2A and 2B provide two magnetic field patterns, such patterns are provided for illustration and not limitation. Accordingly, other systems that utilize alternate methods, frequencies, apparatus, magnetic field patterns, fewer or additional components or alternatives, etc., can be used without departing from the scope of the methods and systems disclosed herein.

For the illustrated systems of FIGs. 1 and 3, temperature measurements can be provided by collecting radiated light using an optical pyrometer or light pipe. The collected radiated light can be analyzed by, for example, a Luxtron model analyzer that

matches the collected light intensities to a block body radiation spectrum to produce a temperature of the silicon wafer. In some embodiments, the spectrum may be modified or scaled to provide an accurate temperature measurement based on the emissivity of silicon.

The EMIH methods and systems can allow a prediction of a magnitude of the induced currents, and hence, the temperature. As provided previously herein, a solution of Faraday's and Ampere's laws can provide a description of the induced current density and the power absorbed, where:

$$P_{ABS} = \frac{\pi a^2 t_w^3 / \left(\delta^4 \sigma\right)}{1 + \left(t_w / \delta\right)^4} H_0^2 \quad , \quad \delta = \sqrt{2/\omega\mu\sigma} \qquad (1)$$

where δ is skin depth, ω is frequency, μ is permeability, σ is conductivity, t_w is thickness, "a" is radius, and H_o is the incident magnetic field. FIG. 4 provides a plot of power absorption based on conductivity according to Equation 1. As FIG. 4 and Equation 1 indicate, the absorbed power increases with conductivity, σ, until a peak absorption is reached. Thereafter, the absorbed power decreases at the same rate of the increase and asymptotes to zero.

The relationship between temperature and conductivity can be instrumental to understanding the FIG. 4 relationship between power absorption and conductivity. FIG. 5 provides the relationship between conductivity and temperature for a variety of substrate doping levels. It is well-known that although

conductivity can be expressed as a product of mobility and carrier density, mobility decreases with temperature due to an increased collision frequency that impedes carrier flow, while carrier density increases with temperature as the increased thermal energy moves carriers from the valence band to the conduction band. Accordingly, as FIG. 5 indicates, conductivity can decrease until the temperature exceeds approximately one-hundred degrees Celsius, during which time collisions impede carrier mobility. As the temperature further increases, the increase in intrinsic carriers can exceed the loss in mobility to allow the conductivity to monotonically increase with temperature. The largest conductivity illustrated in FIG. 5 relates to the peak power absorption level in FIG. 4, and accordingly, when viewing FIGs. 4 and 5 together as a function of increasing temperature, it can be seen that for the smaller illustrated levels of doping, as temperature increases to approximately one-hundred degrees Celsius, conductivity (FIG. 5) decreases and hence power absorption (FIG. 4) is also decreasing, thereby preventing the wafer temperature from increasing. This can otherwise be known as an absorption valley. As the wafer temperature increases beyond this temperature (FIG. 5), however, conductivity increases with temperature, thereby also causing an increase in power absorption (FIG. 4) that can cause a rapid increase in temperature. At approximately five-hundred degrees

Celsius, the intrinsic carrier concentration can greatly exceed the doping such that the conductivity, and hence heating, becomes independent of the substrate doping, and silicon wafers of varying dopant dosages can heat with identical characteristics.

Based on FIG. 4 and 5, and the inference that higher frequency fields (e.g., microwave) can heat more efficiently than lower frequency fields (e.g., RF), in some embodiments, it can be necessary to pre-heat the silicon wafer to a temperature above the absorption valley. In some embodiments, for given power levels, the same wafer temperature can be achieved irrespective of whether one or more wafers are present. Accordingly, batch processing can be equally as effective.

In one embodiment of the methods and systems, B^+ and BF_2^+ ions, at a dose of $10^{15}/cm^3$, were implanted into n-type silicon wafers having resistivities between 10 and 20 ohm-cm over a range of implant energies between 250 eV and 2.2keV. Another sample was implanted at a dose of $10^{15}/cm^2$ using plasma doping (PLAD) (BF_3 gas). The samples were annealed using EMIH, and specifically RF and microwave embodiments, to either 900 or 1000 degrees Celcius in an uncontrolled ambient at atmospheric pressure. FIG. 6 illustrates sheet resistances versus junction depth evaluated at $10^{18}/cm^3$ from SIMS. The solid line in FIG. 6 is the present SEMATECH barrier curve for evaluating improvements in anneal and doping technology. Those of ordinary skill in the

art recognize that data points below the SEMATECH curve indicate a higher percentage of activated dopants and/or a more efficient annealed dopant profile than the SEMATECH standard.

Referring now to FIG. 7, there are plots of SIMS results for the as-implanted and microwave spike annealed PLAD samples. Those with ordinary skill in the art also recognize that a more efficient profile can be obtained by a controlled ambient of oxygen (e.g. 33 to 100ppm) to eliminate the oxygen-enhanced-diffusion effect.

In one embodiment of the methods and systems disclosed herein, sheet resistances were measured for implants of B+ at 250eV and 500eV, and BF2+ at 500eV, 1.1keV, 2.2keV, and 4.5keV, with implant doses of 1.0e15/cm^2, using EMIH annealing, and specifically, RF annealing at 13.96 MHz. In some embodiments, the RF anneal time was thirty seconds to 1000 degrees Celsius and 900 degrees Celsius, while a spike anneal was applied in other embodiments to the same temperatures. In all measured categories of ion beam energy, the thirty-second, 1000 degree temperature RF annealing provided the best sheet resistance, on the order of nearly 300 ohms/sq. to 850 ohms/sq. The remaining experiments described herein provided sheet resistances on the order of 500 ohms/sq to 7000 ohms/sq. Accordingly, although the RF annealing activates the dopant, defects remained in the lattice structure.

In another embodiment where microwave EMIH annealing was performed at 2.45GHz, for thirty-second and spike annealing at 1000 and 900 degrees Celsius, sheet resistance measurements varied on the order of 150 ohms/sq. to 1000 ohms/sq. Once again, defects remained in the lattice structure.

By performing LTRTA (i.e., approximately 500 - 800 degrees Celsius) before or after EMIH annealing, defects in the lattice structure caused by the implantation can be cured without the undesirable diffusion effects caused by traditional RTA methods that necessarily provide silicon temperatures in a range between 900 degrees Celsius and 1200 degrees Celsius to activate the dopant. Accordingly, using the disclosed methods and systems that combine EMIH with low-temperature RTA, a junction and structure having high concentration dopant activation and lattice repair with low diffusion and sheet resistance, can be achieved.

What has thus been described is a method and system to achieve shallow junctions using Electromagnetic Induction Heating (EMIH) that can be preceded or followed by a low-temperature Rapid Thermal Annealing (RTA) process. The methods and systems can use, for example, RF or microwave frequencies, to induce electromagnetic fields that can induce currents to flow within the silicon wafer, thus causing ohmic collisions between electrons and the lattice structure that heat the wafer volumetrically rather than through the surface. Such EMIH

heating can activate the dopant material. Defects in the silicon structure can be repaired by combining the EMIH annealing with a low-temperature (approximately 500 - 800 degrees Celsius) RTA that causes minimal diffusion, thus minimizing the difference between the as-implanted junction depth and the post-annealing junction depth when compared to annealing methods that only use traditional RTA.

The methods and systems described herein are not limited to a particular hardware or software configuration, and may find applicability in many computing or processing environments. The methods and systems can be implemented in hardware or software, or a combination of hardware and software. The methods and systems can be implemented in one or more computer programs executing on one or more programmable computers that include a processor, a storage medium readable by the processor (including volatile and non-volatile memory and/or storage elements), one or more input devices, and one or more output devices.

Although the methods and systems have been described relative to a specific embodiment thereof, they are not so limited. Obviously many modifications and variations may become apparent in light of the above teachings. For example, although the methods and systems illustrated herein referred to silicon semiconductors, other semiconductors, for example, from group IV of the periodic table, can be used, as well as other

semiconductors. Furthermore, although the sample embodiments indicated Boron (B+) as a p-type dopant, the methods and systems can be applied to n-type dopants. Although LTRTA was illustrated as approximately 500-800 degrees Celsius, where the LTRTA can be performed using a furnace, LTRTA can be understood to include an exposure to temperatures less than approximately 800 degrees Celsius. The methods and systems disclosed include providing an oscillating magnetic field to induce the currents in the semiconductor, and although the illustrated methods and systems provided RF and microwave systems, any electromagnetic wave of any frequency that provides a time-varying or oscillating magnetic field can be used. For example, an EMIH embodiment can include a permanent magnet that can be moved to provide a time-varying magnetic field.

Many additional changes in the details, materials, and arrangement of parts, herein described and illustrated, can be made by those skilled in the art. Accordingly, it will be understood that the following claims are not to be limited to the embodiments disclosed herein, can include practices otherwise than specifically described, and are to be interpreted as broadly as allowed under the law.

What is claimed is:

1. A method for annealing a semiconductor structure, the method comprising,

subjecting the semiconductor structure to an oscillating magnetic field, and,

applying a low temperature rapid thermal annealing (LTRTA) process to the semiconductor structure.

2. A method according to claim 1, wherein subjecting includes subjecting to a time-varying electromagnetic field.

3. A method according to claim 1, wherein subjecting includes providing a frequency in the microwave frequency band.

4. A method according to claim 1, wherein subjecting includes providing a frequency in the radio frequency (RF) band.

5. A method according to claim 1, wherein applying a LTRTA includes exposing the semiconductor to a temperature less than approximately 800 degrees Celsius.

6. A method according to claim 1, wherein applying a LTRTA includes exposing the semiconductor to a furnace having a

temperature greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius.

7. A method according to claim 1, wherein applying a LTRTA can precede subjecting the semiconductor to an electromagnetic field.

8. A method according to claim 1, wherein applying a LTRTA includes using a furnace to perform the LTRTA.

9. A method for implanting a dopant in a semiconductor structure, the method comprising,

using ion implantation to implant the dopant in the semiconductor,

activating the dopant using electromagnetic induction heating (EMIH), and,

applying a low-temperature rapid thermal anneal (RTA) process.

10. A method according to claim 9, wherein the dopant is at least one of an n-type dopant and a p-type dopant.

11. A method according to claim 9, wherein activating the dopant using EMIH includes subjecting the dopant to an oscillating magnetic field.

12. A method according to claim 9, wherein activating the dopant includes subjecting the dopant to a time-varying electromagnetic field.

13. A method according to claim 9, wherein activating the dopant includes providing at least one of a Radio Frequency (RF) wave and a microwave frequency.

14. A method according to claim 9, wherein applying a LTRTA includes exposing the semiconductor to a temperature less than approximately 800 degrees Celsius.

15. A method according to claim 9, wherein applying a LTRTA includes exposing the semiconductor to a furnace having a temperature greater than approximately 500 degrees Celsius, and less than approximately 800 degrees Celsius.

16. A method according to claim 9, wherein applying a LTRTA can precede activating the dopant.

17. A method according to claim 9, wherein applying a LTRTA includes using a furnace to perform the LTRTA.

Docket No. VRO-004.01

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

ABSTRACT

A method and system to achieve shallow junctions using Electromagnetic Induction Heating (EMIH) that can be preceded or followed by a low-temperature Rapid Thermal Annealing (RTA) process. The methods and systems can use, for example, RF or microwave frequencies to induce electromagnetic fields that can induce currents to flow within the silicon wafer, thus causing ohmic collisions between electrons and the lattice structure that heat the wafer volumetrically rather than through the surface. Such EMIH heating can activate the dopant material. Defects in the silicon structure can be repaired by combining the EMIH annealing with a low-temperature (approximately 500 - 800 degrees Celsius) RTA that causes minimal diffusion, thus minimizing the difference between the as-implanted junction depth and the post-annealing junction depth when compared to annealing methods that only use traditional RTA.

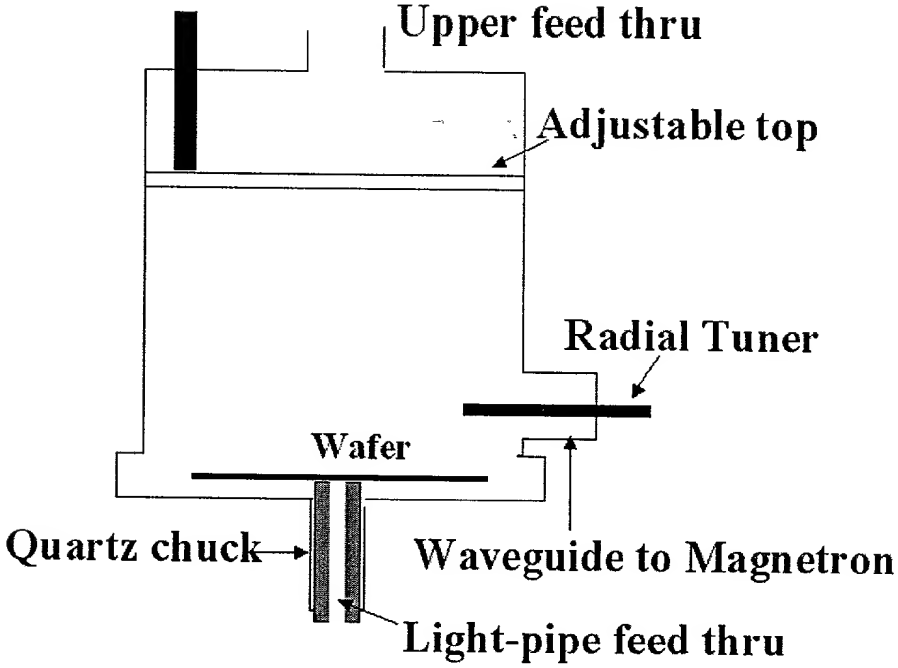
Upper feed thru
Adjustable top
Radial Tuner
Wafer
Quartz chuck
Waveguide to Magnetron
Light-pipe feed thru

FIG. 1

TM011

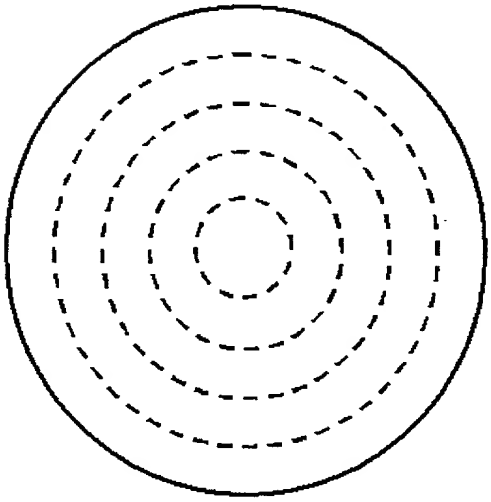

FIG. 2A

TM111

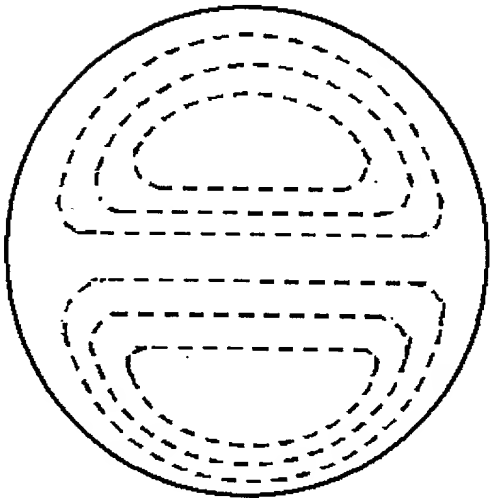

FIG. 2B

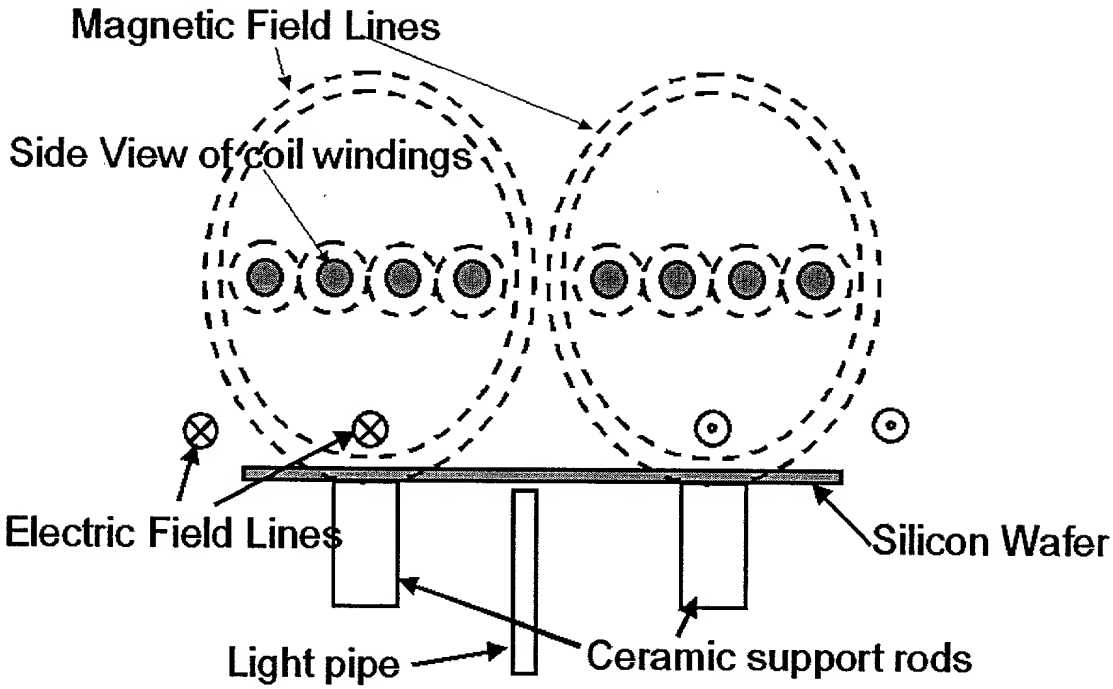
Magnetic Field Lines
Side View of coil windings
Electric Field Lines
Silicon Wafer
Light pipe
Ceramic support rods

FIG. 3

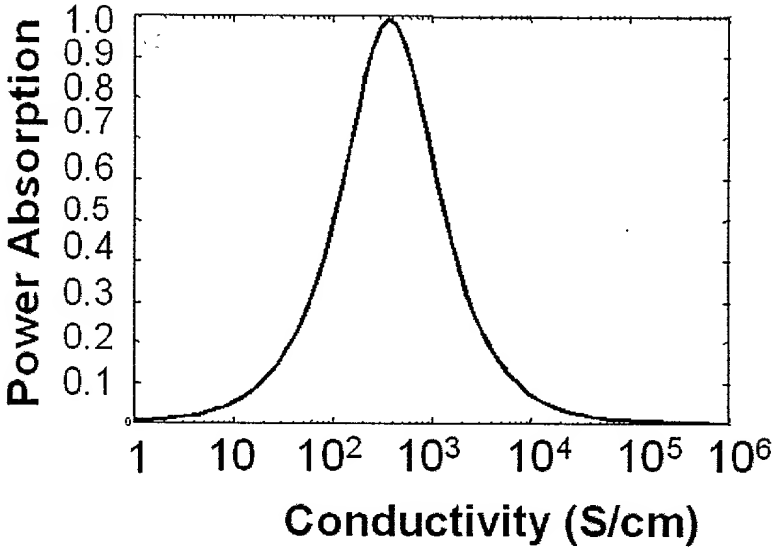
Power Absorption
1.0
0.9
0.8
0.7
0.6
0.5
0.4
0.3
0.2
0.1
0
1
10
10^2
10^3
10^4
10^5
10^6
Conductivity (S/cm)

FIG. 4

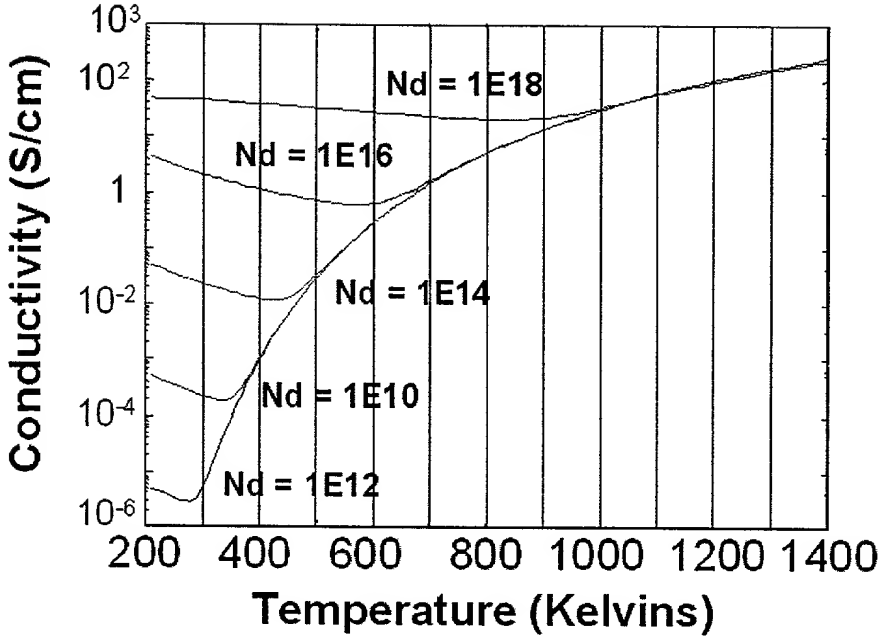
Conductivity (S/cm)
10^3
10^2
1
10^-2
10^-4
10^-6
Nd = 1E18
Nd = 1E16
Nd = 1E14
Nd = 1E10
Nd = 1E12
200
400
600
800
1000
1200
1400
Temperature (Kelvins)

FIG. 5

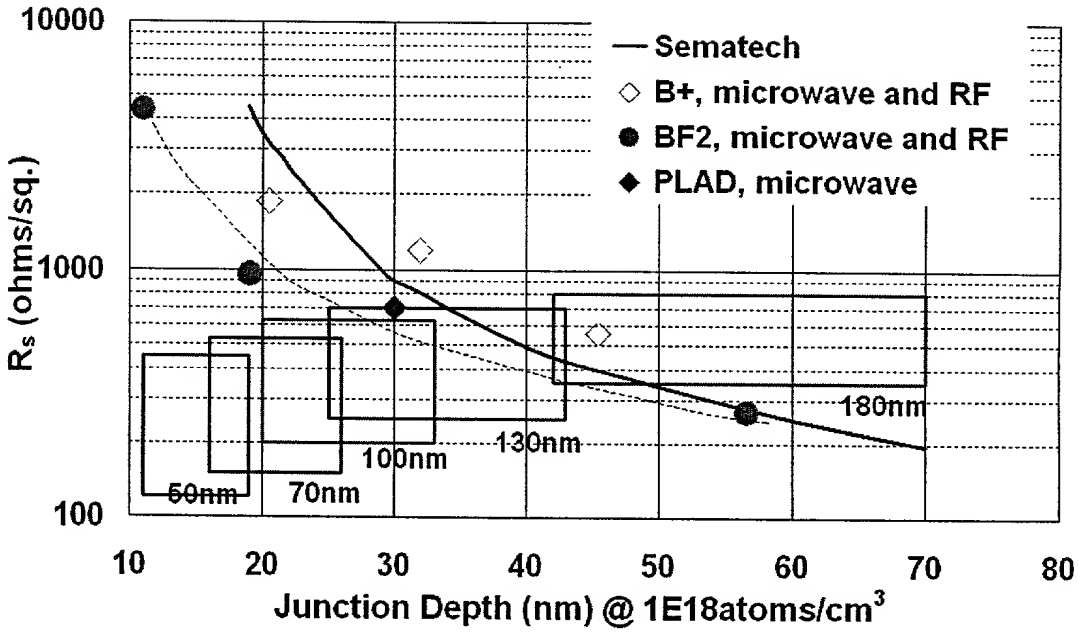
10000
1000
100
R_s (ohms/sq.)
10
20
30
40
50
60
70
80
Junction Depth (nm) @ 1E18atoms/cm^3
Sematech
B+, microwave and RF
BF2, microwave and RF
PLAD, microwave
50nm
70nm
100nm
130nm
180nm

FIG. 6

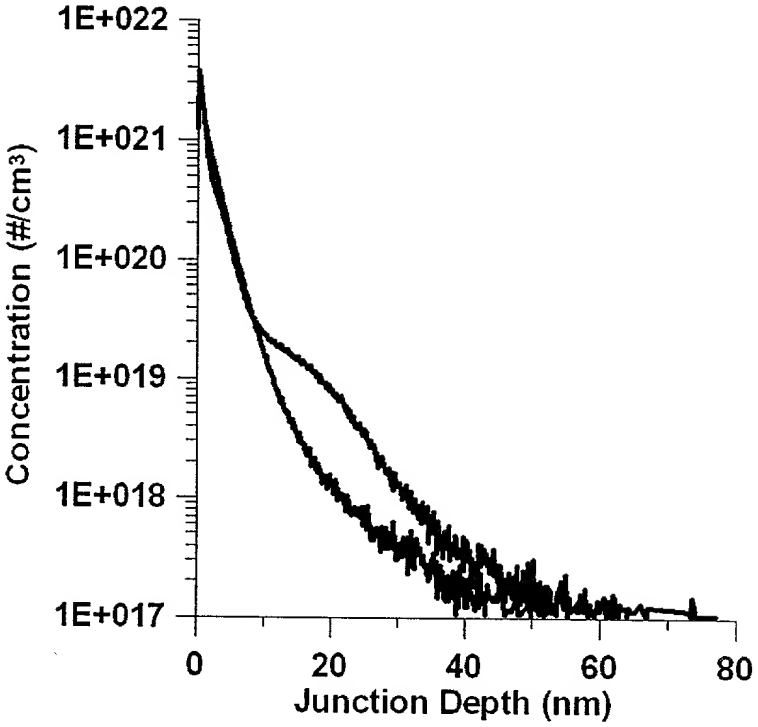
1E+022
1E+021
1E+020
1E+019
1E+018
1E+017
Concentration (#/cm³)
0
20
40
60
80
Junction Depth (nm)

FIG. 7

DECLARATION FOR PATENT APPLICATION

Docket Number VRO-004.01

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

ATHERMAL ANNEALING WITH RAPID THERMAL ANNEALING SYSTEM AND METHOD

the specification of which (check one)

☒ is attached hereto.
☐ was filed on _____ as United States Application Number or PCT International Application Number _____, and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information, which is material to patentability as defined in Title 37, Code of Federal Regulation, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code. § 119(a)-(d) of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No
(Number)	(Country)	(Day/Month/Year Filed)	☐ Yes ☐ No

I hereby claim the benefit under Title 35, United States Code. § 119(e) of any United States Provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status: patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status: patented, pending, abandoned)

I hereby appoint Beth E. Arnold, Reg. No. 35,430; Isabelle Clauss. Reg. No. 47.326; Stephen B. Deutsch, Reg. No. 46,663; William D. DeVaul Reg. No. 42,483: Daniel P. Gaudet. Reg. No. 48,584; Robert W. Gauthier, Reg. No. 35,153; Jason Gish, Reg. No. 42,581; Dana Gordon, Reg. No. 44,719; Robert A. Greenberg, Reg. No. 44,133; Jennifer K. Holmes. Reg. No. 46,778; Scott E. Kamholz, Reg. No. 48,543; David A. Lane, Reg. No. 39,261; W. Hugo Liepmann, Reg. No. 20,407; Jim Olesen, Reg. No. 46.967; Kevin A. Oliver. Reg. No. 42,049; Chinh H. Pham, Reg. No. 39.329; Jeffrey M. Sears, Reg. No. 48,440; Philip C. Swain, Reg. No. 32,376; Kingsley L. Taft, Reg. No. 43,946; John Quisel, Reg. No. 47,874; Anita Varma, Reg. No. 43,221; Sharon Webb, Reg. No. 47,172; John L. Welch, Reg. No. 28,129. and Gary L. Loser, Reg. No. 30,656 as attorneys/agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith.

Address all telephone calls to Gary L. Loser at telephone number (978) 282-2006.

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature: Daniel F. Downey Date: 11/28/01
Residence: 8 Ryan Road, Gloucester, MA 02541 Citizenship: U.S.A.
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